

Reduction in Total Harmonic Distortion by Multilevel Inverters and Passive Filter

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Abstract: The main concept of a multilevel converter is to achieve higher power to use a series of power semiconductor switches with several dc source to perform the power conversion by synthesizing a staircase voltage waveform. In this paper, 3- level and 5- level diode clamped inverter topologies and SPWM technique has been applied to formulate the switching pattern for inverter that minimize the harmonic distortion at the output. A RL passive filter is also introduced for more improvement in results, performed in simulink.

Keywords: Diode Clamped Inverter, Total Harmonic Distortion, SPWM, Passive filter.

1. INTRODUCTION

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. It include an array of power semiconductors and dc voltage sources, the output of which generate voltages with stepped waveforms. The steps being supplied from different DC levels supported by series connected batteries or capacitors[1]. The unique structure of multi- level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. Among various modulation techniques [2] for a multilevel inverter, sin-triangle pulse width modulation (SPWM) is an attractive technique due to the following merits. It proportionally varies the width of each pulse to the amplitude of a sine wave evaluated at the center of the same pulse. It is suitable for MATLAB/SIMULINK implementation. As number of level of diode clamped inverter increases then there is reduction of total harmonics distortion (THD) of inverter output voltage. This is the main advantage of the proposed control method. A RL passive filter is also introduced for improvement in results.

2. MULTILEVEL INVERTER TOPOLOGIES

The basic three types of multilevel topologies used are :(1)Diode clamped multilevel inverters(2)Flying capacitors multilevel inverter or capacitor clamped multilevel inverter (3)Cascaded inverter with separate DC sources.[3]

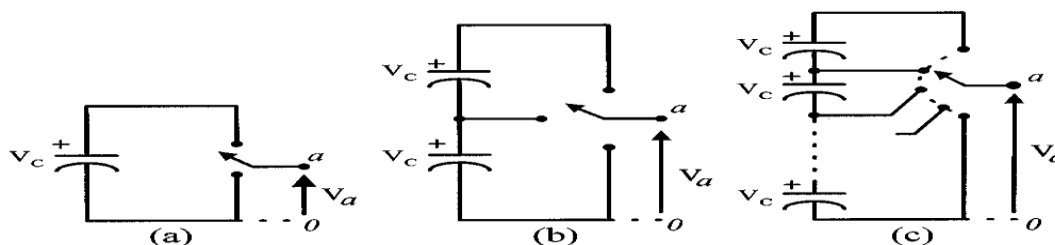


Fig.1. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n level

For research on multi level inverter topologies, a preferred multilevel inverter topology shall have the following characteristics: 1) The level is easy to extend 2) When the number of levels is high enough, the harmonic content is low 3) There is no need for filters 4) Inverter efficiency is high because all devices are switched at the fundamental frequency 5) The control method is simple. Fig .1, shows a schematic diagram of one phase leg of inverters with different number of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions.

3. INVERTER TOPOLOGY

Neutral Point-Clamped Inverter:

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [4]. In general for an N level diode clamped inverter, for each leg, $2(N-1)$ switching devices, $(N-1)*(N-2)$ clamping diodes and $(N-1)$ dc link capacitors are required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement.[5]

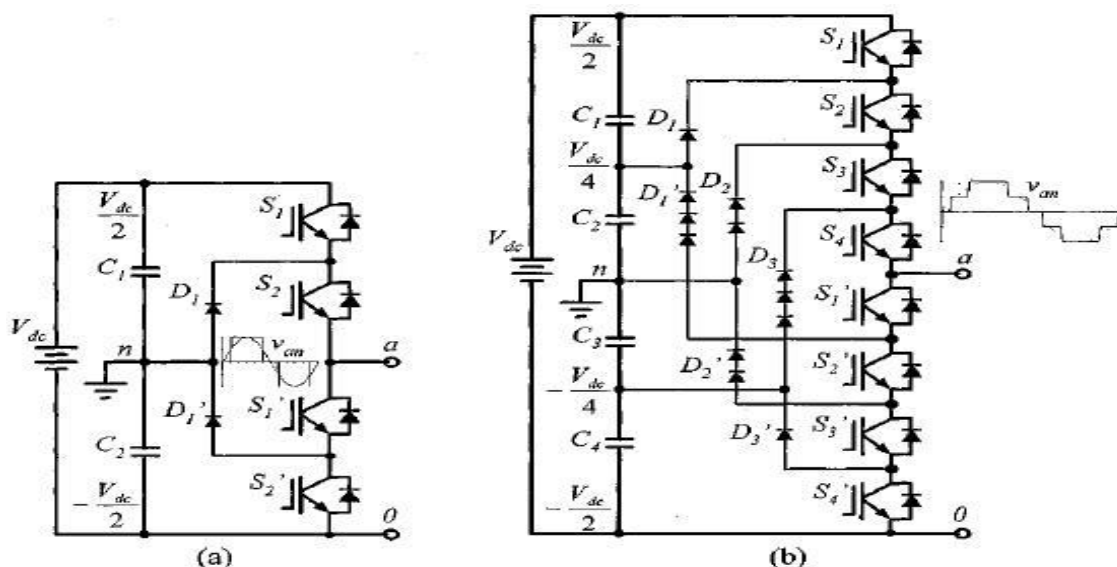


Fig. 2. Diode-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level

A three-level and five-level diode clamped inverter are shown in Fig.2.(a) and Fig.2.(b) respectively.[1]

For a three-level inverter, a set of two switches is on at any given time and in five-level inverter, a set of four switches is on at any given time and so on. Switching states in one leg of three-level and five-level diode clamped inverter are shown in Table-I and Table-II.

TABLE-I SWITCHING STATES FOR THREE LEVEL INVERTER

SWITCH STATUS	STATE	POLE VOLTAGE
$S_1=ON, S_2=ON, S_1'=OFF, S_2'=OFF$	$S=+ve$	$V_{ao}=V_{dc}/2$
$S_1=OFF, S_2=ON, S_1'=ON, S_2'=OFF$	$S=0$	$V_{ao}=0$
$S_1=OFF, S_2=OFF, S_1'=ON, S_2'=ON$	$S=-ve$	$V_{ao}=-V_{dc}/2$

TABLE-II SWITCHING STATES FOR FIVE LEVEL INVERTER

VOLTAGE V_{ao}	SWITCH STATES							
	S1	S2	S3	S4	S1'	S2'	S3'	S4'
$V_{ao}=V_{dc}$	1	1	1	1	0	0	0	0
$V_{ao}=V_{dc}/2$	0	1	1	1	1	0	0	0
$V_{ao}=0$	0	0	1	1	1	1	0	0
$V_{ao}=-V_{dc}/2$	0	0	0	1	1	1	1	0
$V_{ao}=-V_{dc}$	0	0	0	0	1	1	1	1

According to the Table I & Table II, pulses can be generated for all the three phases as explained later.

4. SPWM (SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE)

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers [6]. THD of phase-shifted modulation is much higher than level-shifted modulation. An m-level inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are continuous. There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation: (i) In-phase disposition (IPD), where all carrier waveforms are in phase. (ii) Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero. (iii) Alternate phase opposition disposition (APOD), [7] where every carrier waveform is in out of phase with its neighbour carrier by 180°. Three-level inverter is modelled based on the theoretical concepts. Here the pulse generator is modelled where one reference wave (sine wave) and two carrier waves (triangular wave) are superimposed. Based on the modulation techniques, four pulses are generated by comparing modulating signal with carrier signal. These four pulses are added in order to get an aggregated signal. Pulses which are to be given to the switches in one phase leg of a three level inverter are derived from an aggregated signal. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120 degrees. Five level inverter is modelled in the same way as the three level inverter. The difference here is the number of carrier signal.

5. SWITCHING STRATEGY

Inverter output voltage, $V_{AO} = V_{dc}/2$, When $V_{control} > V_{tri}$, and $V_{AO} = -V_{dc}/2$, When $V_{control} < V_{tri}$. PWM frequency is the same as the frequency of V_{tri} . Amplitude is controlled by the peak value of $V_{control}$ and Fundamental frequency is controlled by the frequency of $V_{control}$. Modulation Index (m) is given by: [8]

$$m = \frac{V_{control}}{V_{tri}} = \frac{\text{peak of } (V_{AO})_1}{V_{dc}/2}$$

Where $(V_{AO})_1$ is the fundamental frequency component of V_{AO}

As shown in fig.3. In Phase Disposition (PD) the converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform and the converter is switched to $-V_{dc}/2$ when the reference is less than both carrier waveforms.

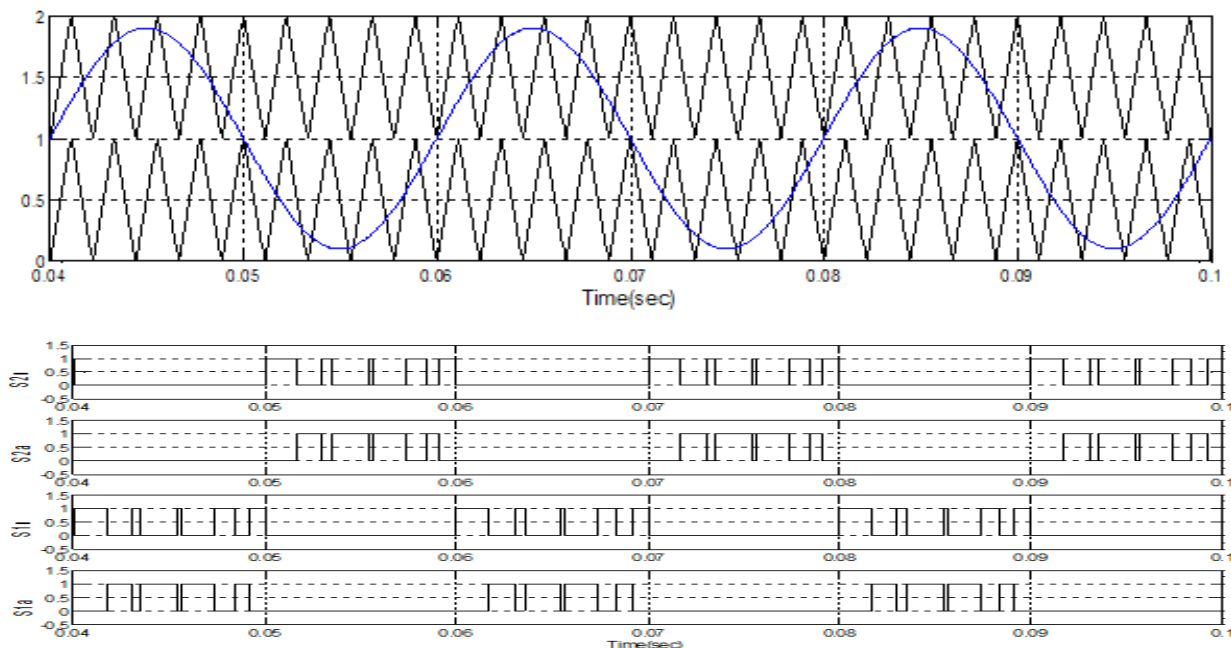


Fig.3. Switching pattern produced using the PD carrier-based PWM scheme

As shown in fig.4. For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero.

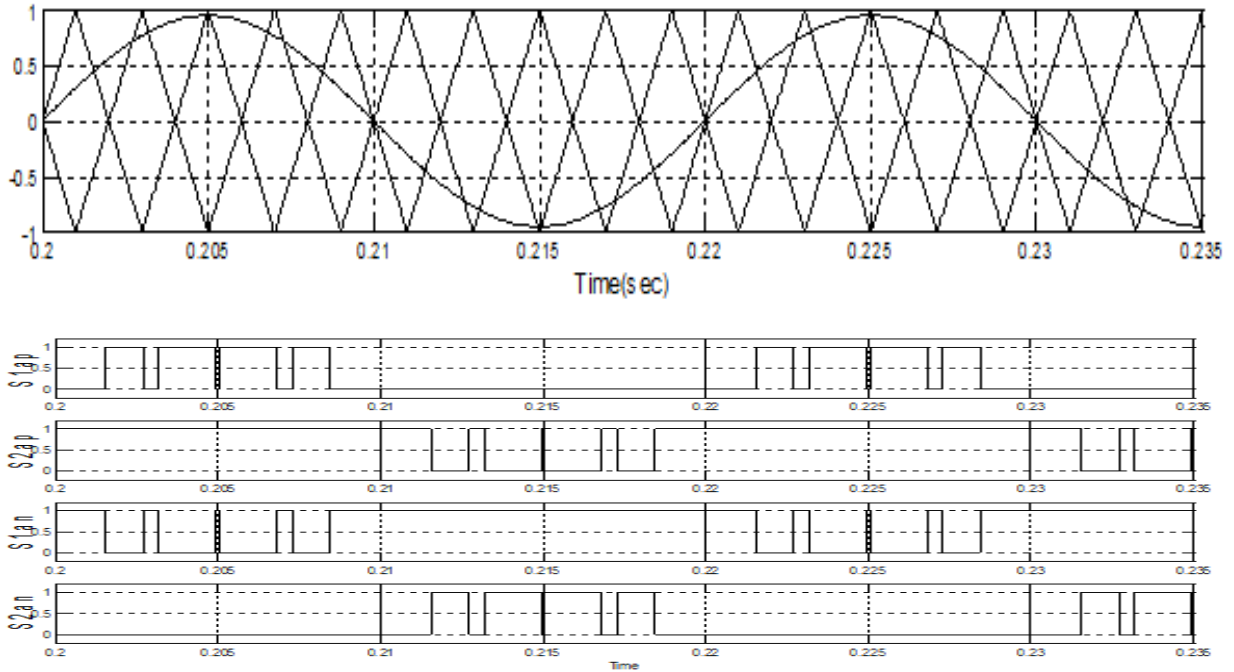


Fig.4. Switching pattern produced using the POD carrier-based PWM scheme: (a) Two triangles and the modulation signal (b) S_{1ap} , S_{2ap} , S_{1an} and S_{2an}

Fig.5. shows the case of alternate phase opposition disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbour carrier by 180° . Since APOD and POD schemes in case of three-level inverter are the same, a five-level inverter is considered to discuss about the APOD scheme. The rules for APOD method, when the number of level $N = 5$, are i) The $N-1=4$ carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbour carrier by 180° . The converter switches to $+V_{dc}/2$ when the reference is greater than all the carrier waveforms. (ii) The converter switches to $V_{dc}/4$ when the reference is less than the uppermost carrier waveform and greater than all other carriers. (iii) The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers. [9]

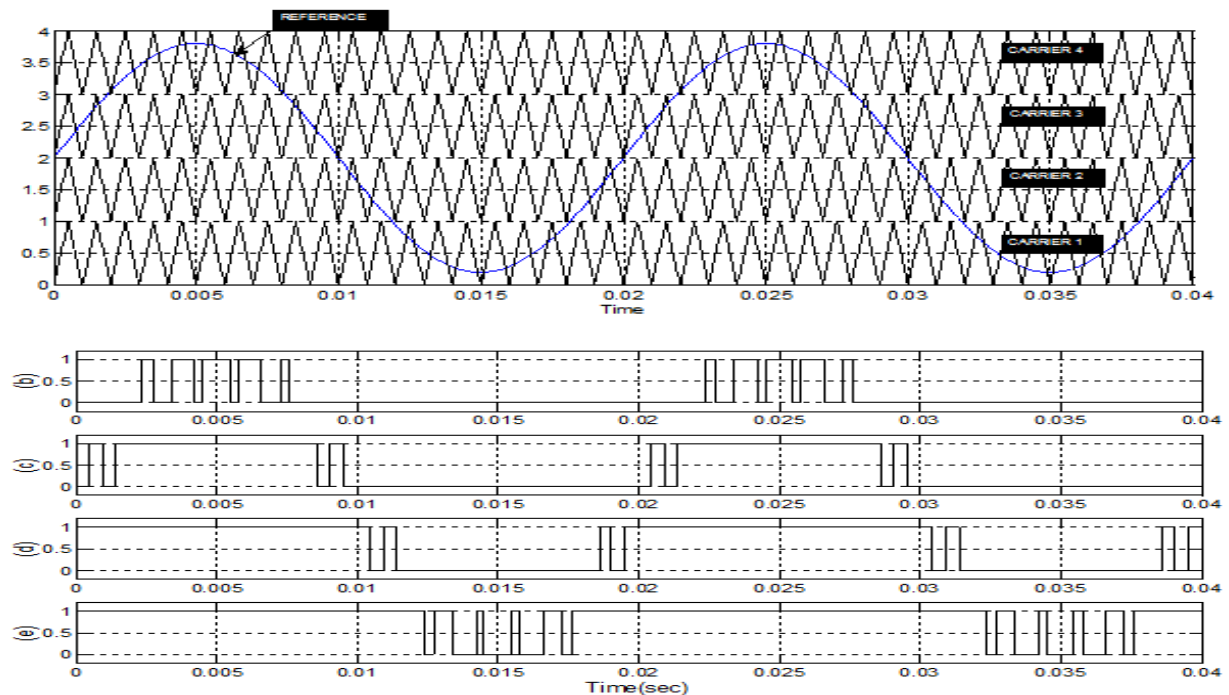


Fig.5. Switching pattern produced using carrier based PWM scheme for a five level inverter using four carrier and a modulating signal

6. PASSIVE FILTER

Filters are frequently used to clean up (i.e. remove high frequency noise) power supplies and remove spurious frequencies from a signal. The simple RL filter is designed to eliminate CMV and harmonic distortions. Filters are mainly classified into three categories: passive, active and hybrid. For, various types of passive filter configuration based on inductors, capacitors and resistors or diodes can be proposed. Passive filters, can suppress the dv/dt value of common-mode differential-mode voltage symmetrically by connecting one terminal of common-mode to the midpoint of dc-link. The ideal harmonic filter can be seen as a device that is capable of completely eliminating reactive current. A low pass RL filter is required at the output terminal of inverter to reduce harmonics generated by the pulsating modulation waveform. While designing R-L filter, the cut-off frequency is chosen such that most of the high order harmonics are eliminated [10].

Series RL Circuit and Series RC Circuit behaves as low pass filter as shown in Fig.6.

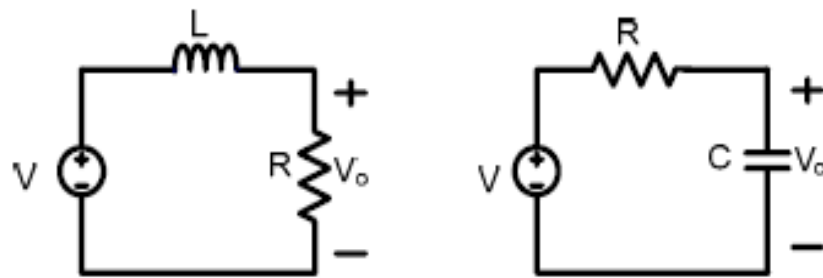


Fig.6. (a) Series RL circuit (b) Series RC circuit

The voltage transfer function of RL circuit is

$$H(s) = \frac{R/L}{S + R/L} \quad \text{Eq...}(1)$$

7. SIMULATION

The fig. 6 shows the MATLAB/SIMULINK MODEL for 3-level neutral clamped multilevel inverter with PWM technique. The fig.7 shows the subsystem diagram of 3-level neutral clamped multilevel inverter. It consists of 12 MOSFET switches, 6 clamping diodes which are connected with single DC source. The fig.8 shows the matlab/simulink model of three phase 5-Level neutral clamped multilevel inverter. The fig.9 shows the subsystem diagram of 5-level neutral clamped multilevel inverter. This model consists of 24 MOSFET switches, 12 clamping diodes and 4 DC link capacitors with single DC source are connected in order to form 5-level neutral clamped multilevel inverter. The fig. 10 shows the multicarrier wave generation arrangement of the proposed converter.

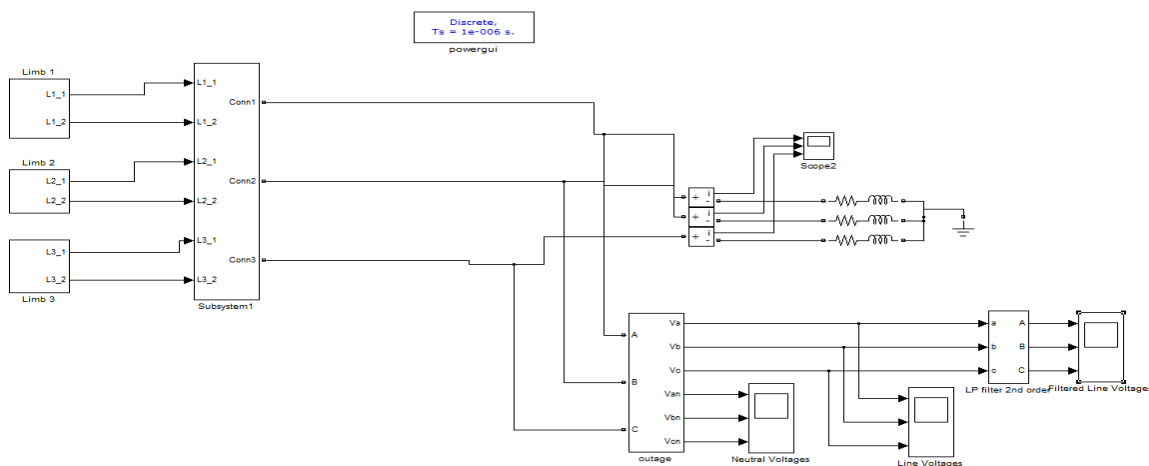


Fig.6.Simulation circuit of Three-Level diode-clamped inverter

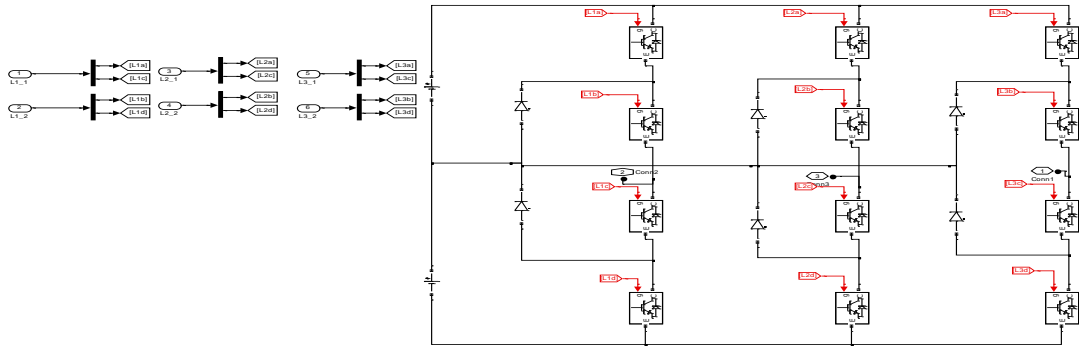


Fig.7.Subsystem diagram of Three-Level diode-clamped inverter

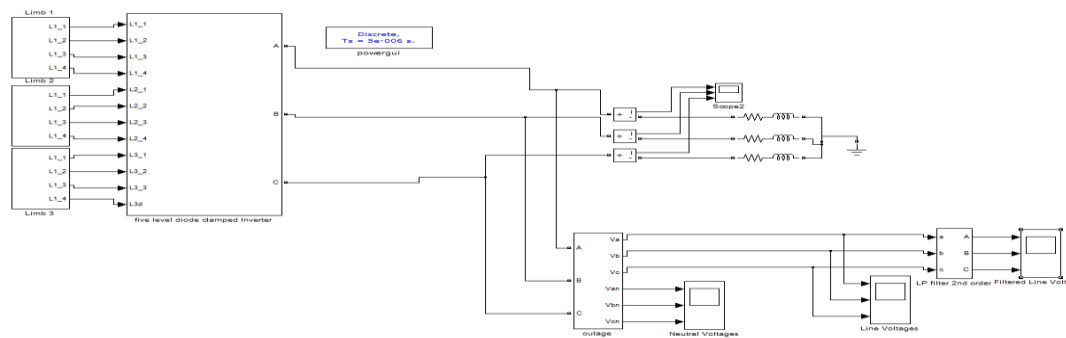


Fig.8.Simulation circuit of Five-Level diode-clamped inverter

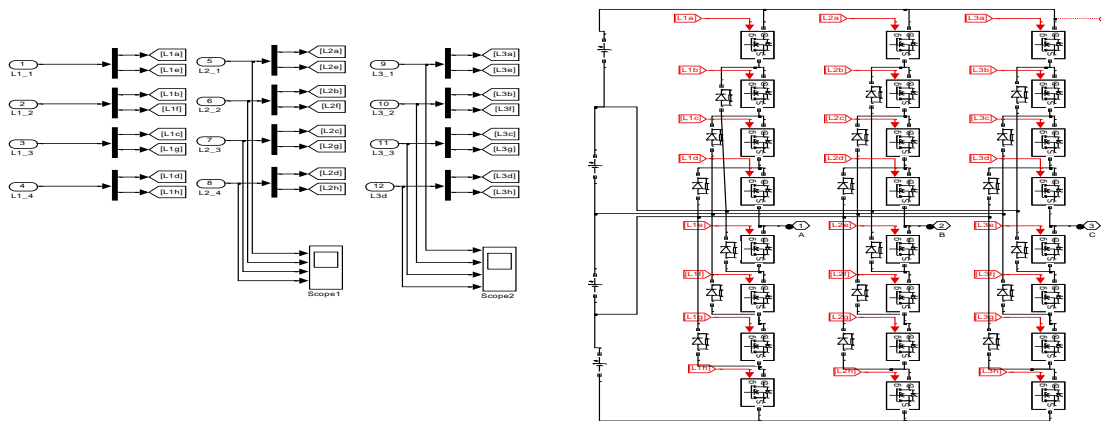


Fig.9.Subsystem diagram of Five-Level diode-clamped inverter

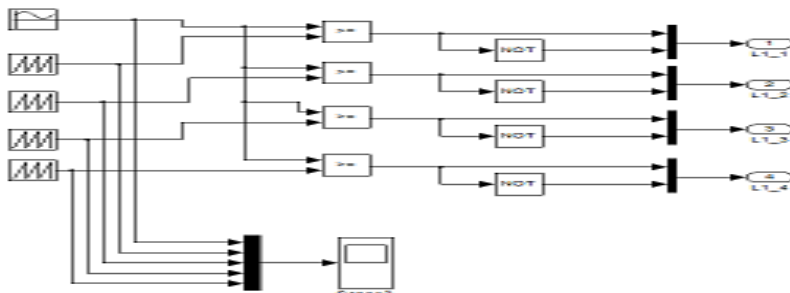


Fig.10. Multicarrier wave generation arrangement

8. SIMULATION RESULTS

To verify the proposed scheme, MATLAB/SIMULINK software is used. Simulation results show that as inverter level increases from 3-level to 5-level total harmonic distortion reduces to 17.37% from 43.63%. Line voltage and line current waveform for RL load for three-level inverter ,Line voltage and Line current waveform for Five -level inverter and comparison of THD of three-level and five level diode clamped inverter is observed.

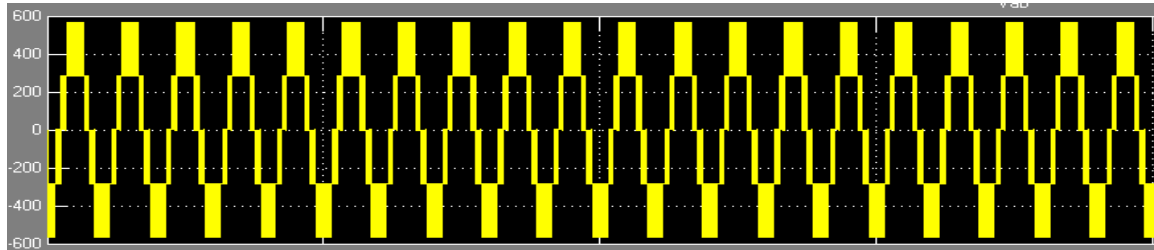


Fig.11. Line voltage of 3-level DCMI with SPWM

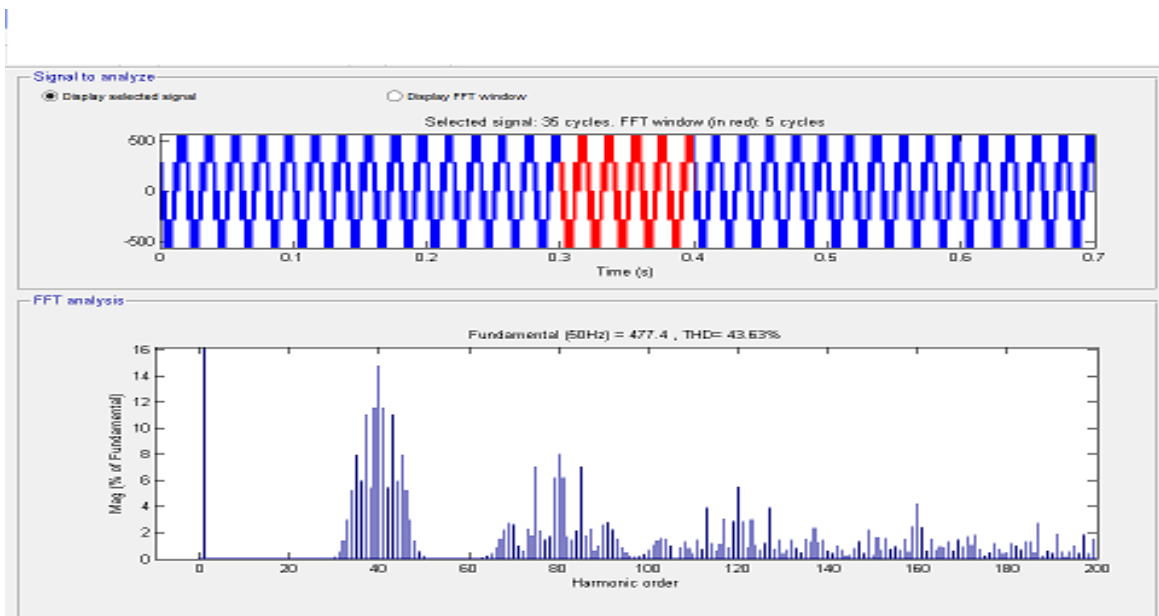


Fig. 12. Line Voltage and Harmonic Spectrum of 3-level Diode clamped multilevel inverter

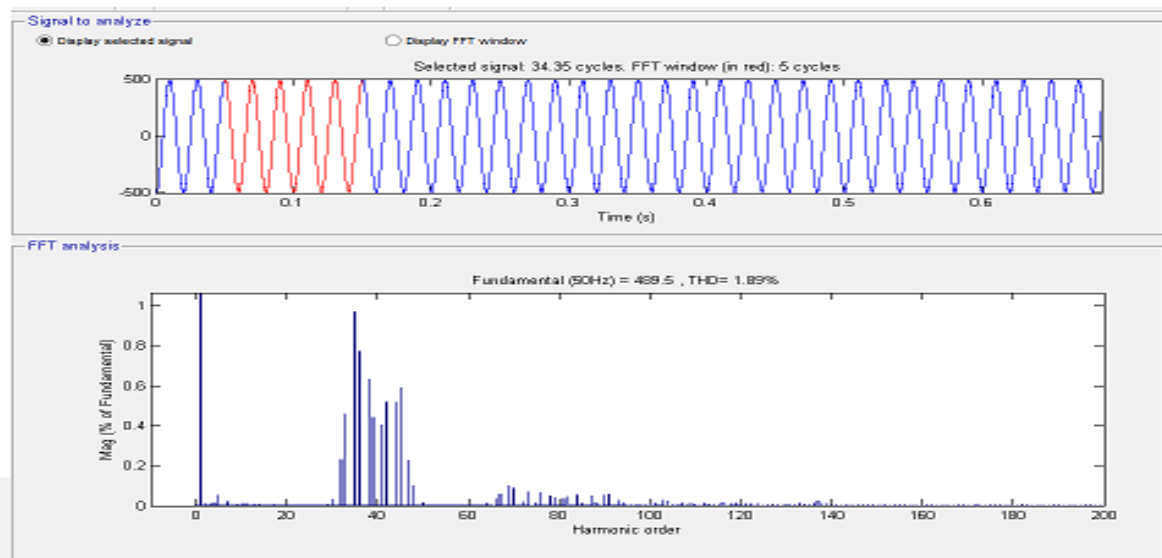


Fig.13. Line Voltage and Harmonic Spectrum of 3-level Diode clamped multilevel inverter with passive filter.

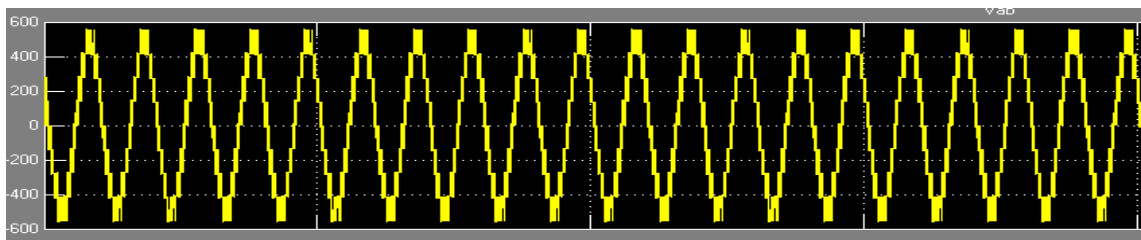


Fig.14. Line voltage of 5-level DCMI with SPWM

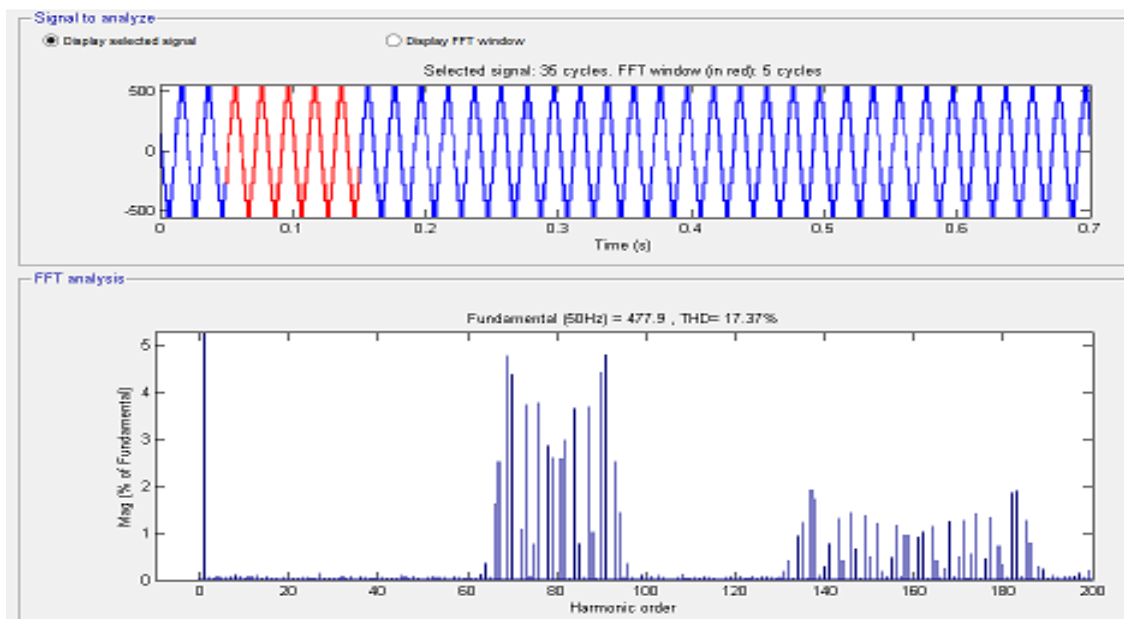


Fig.15. Line Voltage and Harmonic Spectrum of 5-level Diode clamped multilevel inverter

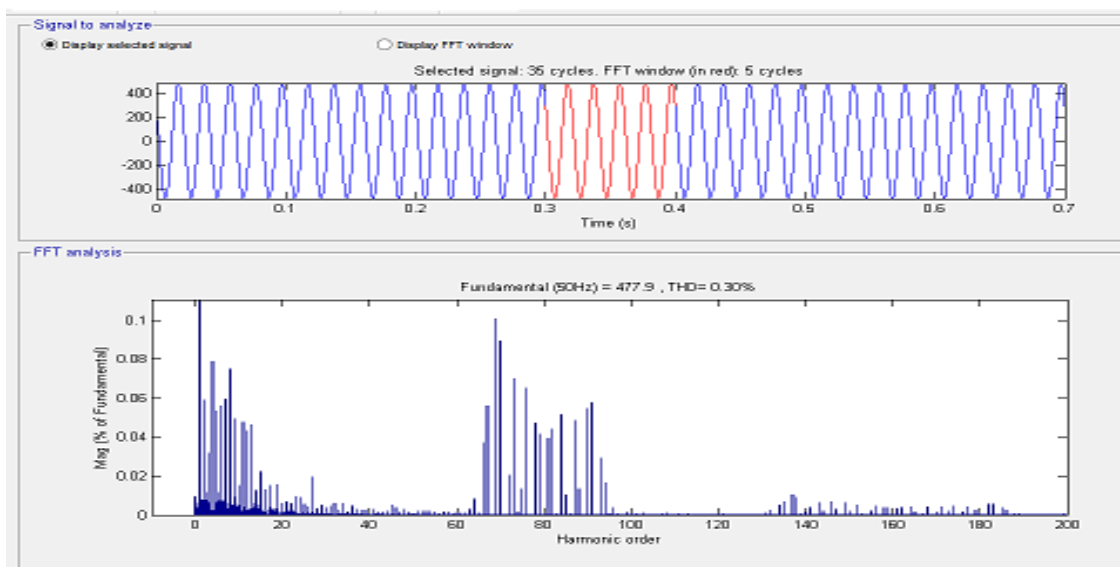


Fig.16. Line Voltage and Harmonic Spectrum of 5-level Diode clamped multilevel inverter with passive filter

The proposed inverter scheme was simulated using Simulink /matlab 2009. Parameters used for simulation are as follows: $f_m = 50\text{Hz}$, $f_c = 10\text{kHz}$. . DC voltage of the inverter for three level is $V_{dc} = 282.5\text{V}$ and for five level $V_{dc} = 141.2\text{V}$. Load is

assumed to be of RL load where $R=15$ Ohms, $L=24.2$ mH . The total harmonic distortion analysis has been done for voltages and currents of three level and five level inverter and their values are compared and shown in Table-III .It is observed that by using the Passive Filter load side harmonics are reduced upto 1.89% for three-level Diode clamped multilevel Inverter and 0.3% five-level Diode clamped multilevel inverter.

TABLE-III REDUCTION OF THD BY VARYING INVERTER LEVEL

Parameters (line voltages and phase currents)	3-level (% THD values)	5-level (% THD values)	3-level with filter (% THD values)	5-level with filter(% THD Values)
V_{ab}	43.63	17.37	1.89	0.30
V_{bc}	43.65	17.37	2.12	0.30
V_{ca}	35.32	17.32	2.12	0.29
I_a	1.74	0.41	0.41	0.41
I_b	1.99	0.41	0.41	0.41
I_c	1.74	0.41	0.41	0.41

9. CONCLUSION

In this paper SPWM technique is proposed for three-level and five-level Diode clamped inverter. The comparative THD analysis of a three phase 3-level and 5-level neutral clamped multilevel inverter is presented in this paper. The various multicarrier PWM technique like Phase disposition (PD), Phase opposition disposition (POD), and Alternative phase opposition disposition (APOD) PWM techniques are applied to the three-level and five-level diode clamped inverter. The main feature of the modulation scheme lies in its ability to eliminate the harmonics in inverter output voltage and output current. The lower order harmonics were considerably reduced in the SPWM technique. By increasing the number of levels, the THD will be decreased but on the other hand cost and weight will be increased as well. Also since the switching angles for switches are not the same, the drive circuit for each switch is separate from other switches. An Passive filter is also introduced for further improvement in results.

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